DETAILED ACTION

Response to Amendment

1. This office action has been issued in response to the amendment filed 09/08/09. Claims 1-7, 12 are pending in this application. Applicant's arguments have been carefully considered, but are not persuasive in view of the prior art as applied to a broadest reasonable interpretation of the claims and/or moot in view of new grounds of rejection. The examiner appreciates Applicant's effort to distinguish over the cited prior art by amending the claims in an attempt to distinguish or clarify the claimed invention, however, upon further consideration and/or search, the claims remain unpatentable over the cited prior art. All claims pending in the instant application remain rejected and clarification and/or elaboration regarding why the claims are not in condition for allowance will hereafter be provided in order to efficiently further prosecution. Accordingly this action has been made FINAL.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. **Claims 1, 2, 6 are rejected** under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention because the claims lack one or more limitations pertaining to completion notifying means for notifying a first device that a data communication for a second buffer has been completed, and, update means for updating a second data buffer for which a data communication has been completed in accordance with a notification by said completion notifying means – such that it would not be possible to determine whether or not a second buffer has been updated or not as implicitly required by the last limitations of the instant

claims. As such, a broadest reasonable interpretation of the instant claims includes using two data buffers, updating the two buffers, and reusing them – as disclosed by the cited art.

5. **Claim 12 is rejected** under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention because the claim specifies a completion message indicating that a data communication for the first and second data buffers has been completed, but then goes on to contradict this limitation by suggesting that a data communication for the second data buffer has not been completed. Moreover, since the completion message is received for both buffers, but only the first buffer is updated and the second is not (at least implicitly), the examiner is left to assume that the second buffer is not updated irrespective of the reception of a completion message and therefore is unresponsive to the system of which it is a part. Assuming the buffer is updated in accordance with the completion message (although this is not claimed), a broadest reasonable interpretation of the instant claims includes using two data buffers, updating the two buffers, and reusing them – as disclosed by the cited art.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.

2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

8. **Claims 1-7, 12 are rejected** under 35 U.S.C. 103(a) as being unpatentable over Leong et al. (US Patent # 2003/0182503) in view of Asano et al. (US Patent # 6,820,187).

With respect to **independent claims 1, 2, 6, 12** Leong discloses: An information processing system/method/apparatus including

first and second devices which connect to each other via a communication control bus [*client 175, storage system 105, disk array 115 or any combination thereof including elements 145, 150, 155 (Leong – Fig. 1) – all elements are interconnected via bus/intercommunication means*];

wherein said first device comprises first and second data buffers [*storage is comprised of a plurality of buffers, wherein a data buffer is understood to be some unit amount of storage operable to store data therein (Leong Fig. 1, paragraph 0004)*] and transmission unit/means for transmitting to said second device, a command block [*a single (macro-command/request) I/O task is transmitted via transmission means (Leong Fig. 1) from a requestor to one or more targets in the form of a plurality of lower-level asynchronous I/O tasks (micro-commands) (Leong abstract, paragraphs 0014, 0046-0047, 0055)*] which designates processing to be performed with said first data buffer and processing to be performed with said second data buffer [a *(macro-command/request) I/O task will designate some processing to be performed for the plurality of data buffers (storage areas) (Leong – abstract, paragraphs 0014, 0046-0047, 0055 and also Fig. 3, 5, paragraphs 0057-0070). Storage system 105 working in conjunction with any of the managers and/or software modules in memory 125 is operable to execute a command/request by interacting with a plurality of storage devices such as those in disk array 115 (Leong – abstract, Fig. 1, paragraph 0020)*];

wherein said second device comprises completion notifying means for notifying said first device that a data communication for said first data buffer has been completed [*as (micro) I/O tasks, (dealing*

with individual data buffers or storage areas) complete, the system issues messages/notifications of incremental progress to ensure efficient forward progress of larger tasks (Leong –abstract, paragraph 0050-0052, 0065-0066, 0069)];

wherein said first device further comprises update means for updating said first data buffer for which the data communication has been completed, in accordance with the notification by said completion notifying means [*Leong's invention (including first and second devices) comprises update means to update storage areas for which there are no outstanding (completion notification not yet received) subordinate I/O tasks, and for not updating (via conditional task suspension) storage areas for which outstanding (completion notification not received) I/O task(s) exist or is/are in the process of completing (Leong – Fig. 4, 5) – for example a write command executed by a child I/O task*].

wherein said transmission means transmits, to said second device, another command block which designates processing to be performed with said first data buffer updated by said update means and processing to be performed with said second data buffer which is not updated by said update means, even if the communication for said second data buffer has not been completed [*considering the 35 U.S.C. 112 issues mentioned above - any number of commands are issued to the second device, each command designates processing to be performed with data residing in any number of data buffers; once a first round of processing for the first data buffer is complete, two data buffers used in a current/previous round of processing may be used for subsequent processing independent of, or with no regard for whether a second data buffer's processing has been completed; note that the first and second data buffers may be accessed by two I/O tasks which do not have corresponding child I/O tasks and thus will not be suspended in order to wait for any child tasks to complete (Leong Fig. 4-5, paragraph 0094)*].

Leong does not **explicitly** disclose (hardware) devices comprising completion notifying (hardware) means for notifying each other of the completion of (data access) requests, but rather discloses his invention more so in the context of tasks notifying other tasks of the completion of data access

requests. It is understood that the tasks are operating via the underlying hardware devices such that the limitation in question is understood to be at least implicitly taught or strongly suggested by the cited disclosure of Leong. Accordingly, it is noted that one of ordinary skill may understand Leong's disclosure to anticipate the instant claims.

Nevertheless, in the same field of endeavor Asano teaches a multiprocessor system wherein hardware devices (processors, and memory controllers) (*Asano Fig. 1, 6-7, 16*) operate in a cooperative multiprocessing environment in which commands/requests may be issued executed asynchronously (*Asano Col 5 lines 45-51*), and without waiting for a response to a previously sent command; wherein hardware means (counters and/or status flags) are provided for notifying other hardware elements of command/request initiated completion of a data communication (*Asano – abstract, Fig. 1, Col 6 lines 12, Col 10 lines 20-30*).

Therefore Leong in view of Asano disclose all limitations of the instant claim(s) including:

wherein said first device further comprises update means for updating, using another command block, the one data buffer for which the data communication has been completed in accordance with the notification by said completion notifying means without updating the other data buffers among the first and second data buffers [*counters/flags are only updated for those data transfer commands that have had notification so completion issued on their behalf (Asano – abstract, Fig. 1, Col 6 lines 12, Col 10 lines 20-30)*].

It would have been obvious to one having ordinary skill in the art at the time of the invention to allow hardware devices to notify each other as opposed to software constructs/mechanisms doing the same because this would be advantageous in terms of implementation flexibility (*Leong - 0035*) and moreover would have been within the purview of the artisan since it is known in the art that hardware and software are logically equivalent *(evidenced by Tanenbaum ("Structured Computer Organization, 3rd ed. 1990," section 1.4, page 11, hardware and software are logically equivalent)*. Therefore it is understood

that the tasks, and their underlying hardware perform the functionality of the claimed completion notifying means since although the instant claim limitation is directed toward hardware means for notifying a (hardware) device of completion of a data communication, the operations to be performed by the (hardware) means correspond to the operations performed by the tasks and/or underlying hardware supporting the tasks (as disclosed by Leong), and one of ordinary skill in the art would realize that a (software) task performing a set of operations would read upon a hardware element performing those same set of operations.

With respect to **dependent claim 3** as applied to claim 2 above Leong discloses the two devices are connected via a communication control bus complying with IEEEI394 [*The examiner is taking official notice that connecting to storage via IEEE 1394 would have been obvious to one having ordinary skill in the art at the time of the invention. Implementing this feature in the invention of Leong would have been obvious to one having ordinary skill in the art because connecting to external storage via IEEE 1394 is old and well known in the art (as evidenced by Palatov US PGPub # 2001/0029583 - page 8 paragraph 0098, page 14 paragraph 0164), and one of ordinary skill would be motivated to connect to external storage via IEEE1394 because an IEEE1394 interface is a known serial high speed interface for storage devices, and also because Leong suggests this limitation by disclosing coupling storage disks to a storage system over an I/O interconnect arrangement, such as a conventional high-performance, Fibre Channel serial link (Leong – paragraph 0037)*].

With respect to **dependent claims 4, 7** as applied to claims 2, 6 above Leong discloses transmitting the command block [*Leong – paragraph 0046*] which contains a plurality of pieces of identification information respectively indicating the first and second data buffers, and commands respectively for the first and second data buffers [*an exemplary I/O task includes eight parameters, which include identification information respectively indicating the first and second data buffers or storage*

areas, and commands respectively for the first and second data storage areas (Leong – paragraph 0047 - 0049)].

With respect to **dependent claim 5** as applied to claim 2 above Leong discloses writing data to the first data buffer or reading data from the first data buffer [*Leong – paragraph 0020*].

Response to Arguments

9. Applicant's arguments filed 09/08/09 have been fully considered but are not persuasive in view of the prior art and/or moot in view of new ground(s) of rejection. All claims pending in the instant application remain rejected. Please note that any rejections/objection not maintained from the previous Office Action have been rectified either by applicant's amendment and/or persuasive argument(s).

Applicant argues that the cited references do not teach the newly worded limitations. The above rejections have been adjusted to correspond to the newly worded limitations.

Conclusion

When responding to the office action, **any new claims and/or limitations should be accompanied by a reference as to where the new claims and/or limitations are supported in the original disclosure**.

THIS ACTION IS MADE FINAL. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action

is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Marwan Ayash whose telephone number is 571-270-1179. The examiner can normally be reached on Mon-Fri 11am-8pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sanjiv Shah can be reached on (571)272-4098. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Sanjiv Shah/
Supervisory Patent Examiner, Art Unit 2185
10/20/09

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